IS65C256AL
IS62C256AL

32K x 8 LOW POWER CMOS STATIC RAM

FEBRUARY 2020

FEATURES

- Access time: 25 ns, 45 ns
- Low active power: 200 mW (typical)
- Low standby power
  - — 150 µW (typical) CMOS standby
  - — 15 mW (typical) operating
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V power supply
- Lead-free available
- Industrial and Automotive temperatures available

DESCRIPTION

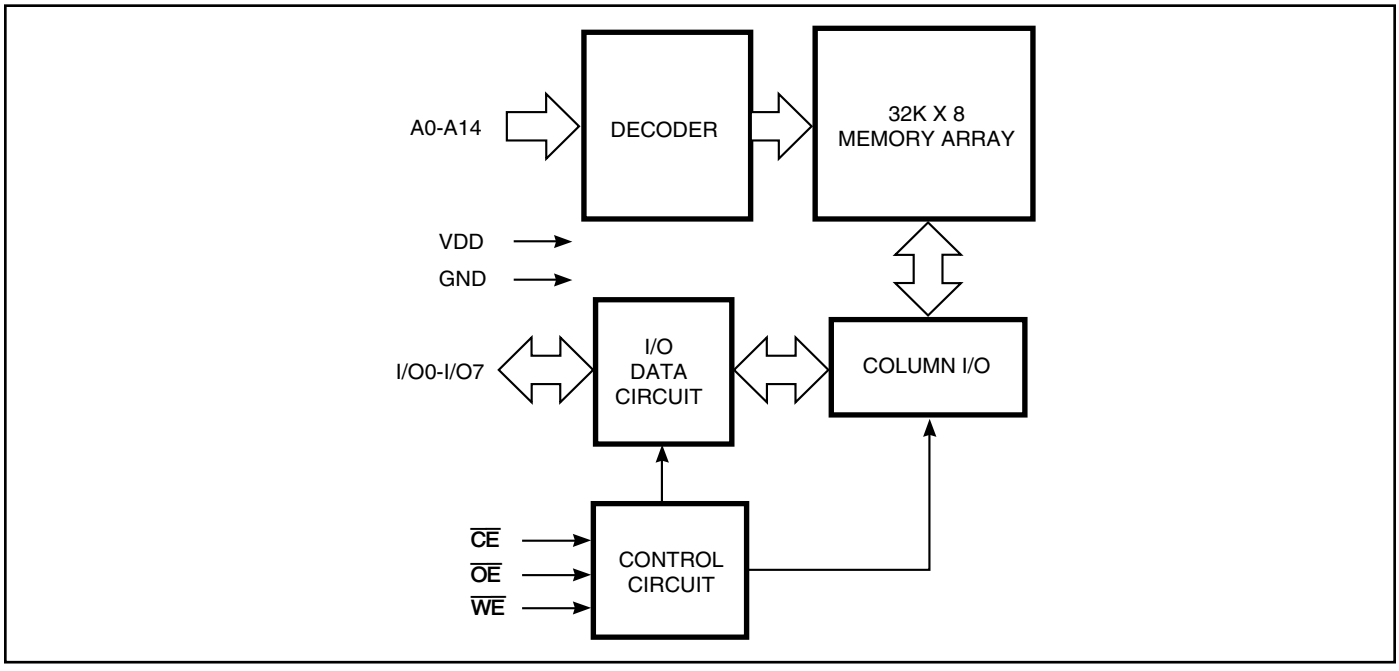
The *ISSI* IS62C256AL/IS65C256AL is a low power, 32,768 word by 8-bit CMOS static RAM. It is fabricated using *ISSI*'s high-performance, low power CMOS technology.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 150 µW (typical) at CMOS input levels.

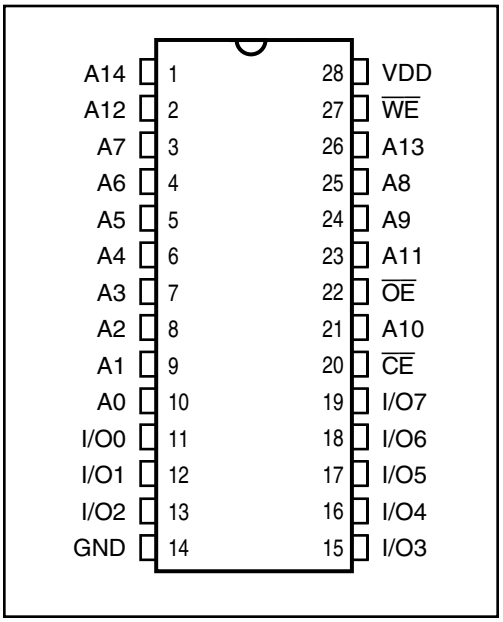
Easy memory expansion is provided by using an active LOW Chip Select ($\overline{CE}$) input and an active LOW Output Enable ($\overline{OE}$) input. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS62C256AL/IS65C256AL is pin compatible with other 32Kx8 SRAMs in plastic SOP or TSOP (Type I) package.

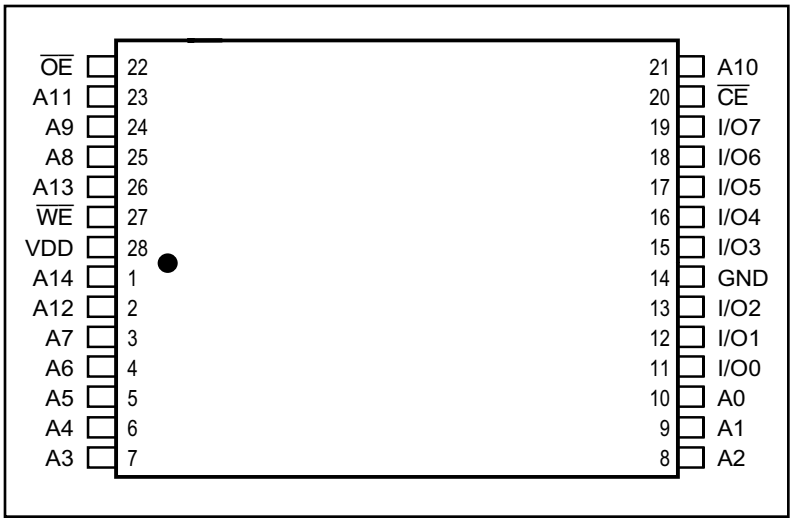
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
28-Pin SOP



PIN CONFIGURATION
28-Pin TSOP



PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Part No.	Range	Ambient Temperature	V_{DD}
IS62C256AL	Commercial	0°C to +70°C	5V ± 10%
IS62C256AL	Industrial	–40°C to +85°C	5V ± 10%
IS65C256AL	Automotive	–40°C to +125°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 2.1 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com.	–1	1	µA
			Ind.	–2	2	
			Auto.	–10	10	
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	Com.	–1	1	µA
			Ind.	–2	2	
			Auto.	–10	10	

Note: 1. V_{IL} = –3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-25 ns Min.	-25 ns Max.	-45 ns Min.	-45 ns Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL}	Com.	—	15	—	15	mA
		I_{OUT} = 0 mA, f = 0	Ind.	—	20	—	20	
			Auto.	—	25	—	25	
I_{CC2}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL}	Com.	—	25	—	20	mA
		I_{OUT} = 0 mA, f = f_{MAX}	Ind.	—	30	—	25	
			Auto.	—	35	—	30	
			typ. [2]	15		12		
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max.,	Com.	—	100	—	100	µA
		V_{IN} = V_{IH} or V_{IL}	Ind.	—	120	—	120	
		$\overline{CE}$ ≥ V_{IH}, f = 0	Auto.	—	150	—	150	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max.,	Com.	—	15	—	15	µA
		$\overline{CE}$ ≥ V_{DD} – 0.2V,	Ind.	—	20	—	20	
		V_{IN} ≥ V_{DD} – 0.2V, or	Auto.	—	50	—	50	
		V_{IN} ≤ 0.2V, f = 0	typ. [2]	5		5		

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5.0V, T_A = 25°C and not 100% tested.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-25 ns Min.	-25 ns Max.	-45 ns Min.	-45 ns Max.	Unit
t_{RC}	Read Cycle Time	25	—	45	—	ns
t_{AA}	Address Access Time	—	25	—	45	ns
t_{OHA}	Output Hold Time	2	—	2	—	ns
t_{ACS}	$\overline{CE}$ Access Time	—	25	—	45	ns
t_{DOE}	$\overline{OE}$ Access Time	—	13	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	12	0	20	ns
t_{LZCS}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t_{HZCS}[2]	$\overline{CE}$ to High-Z Output	0	12	0	20	ns
t_{PU}[3]	$\overline{CE}$ to Power-Up	0	—	0	—	ns
t_{PD}[3]	$\overline{CE}$ to Power-Down	—	20	—	30	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

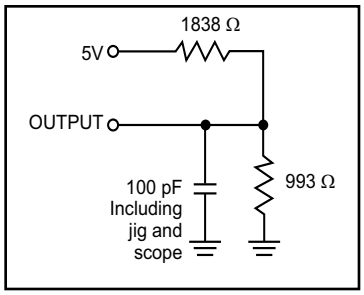


Figure 1.

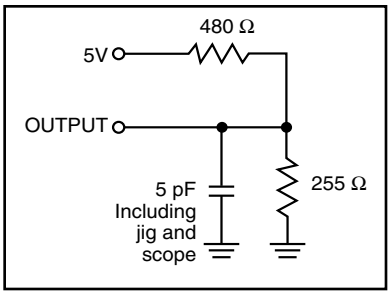
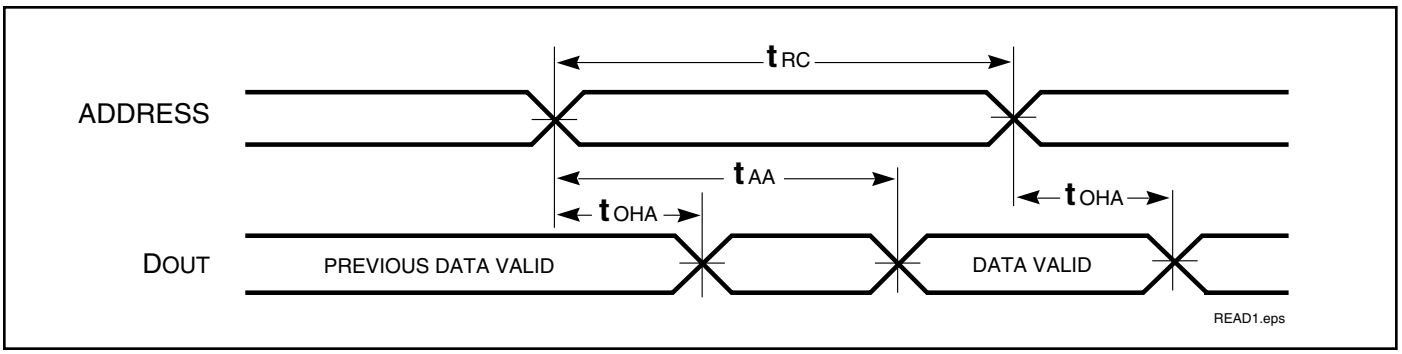


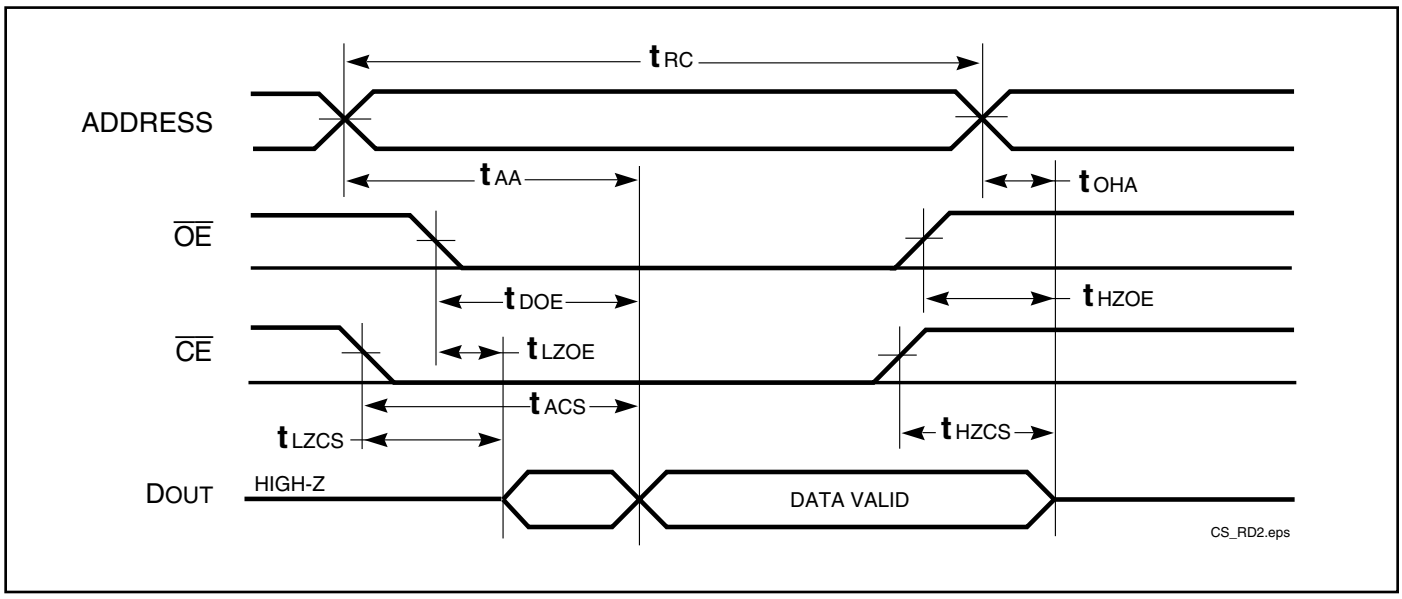
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

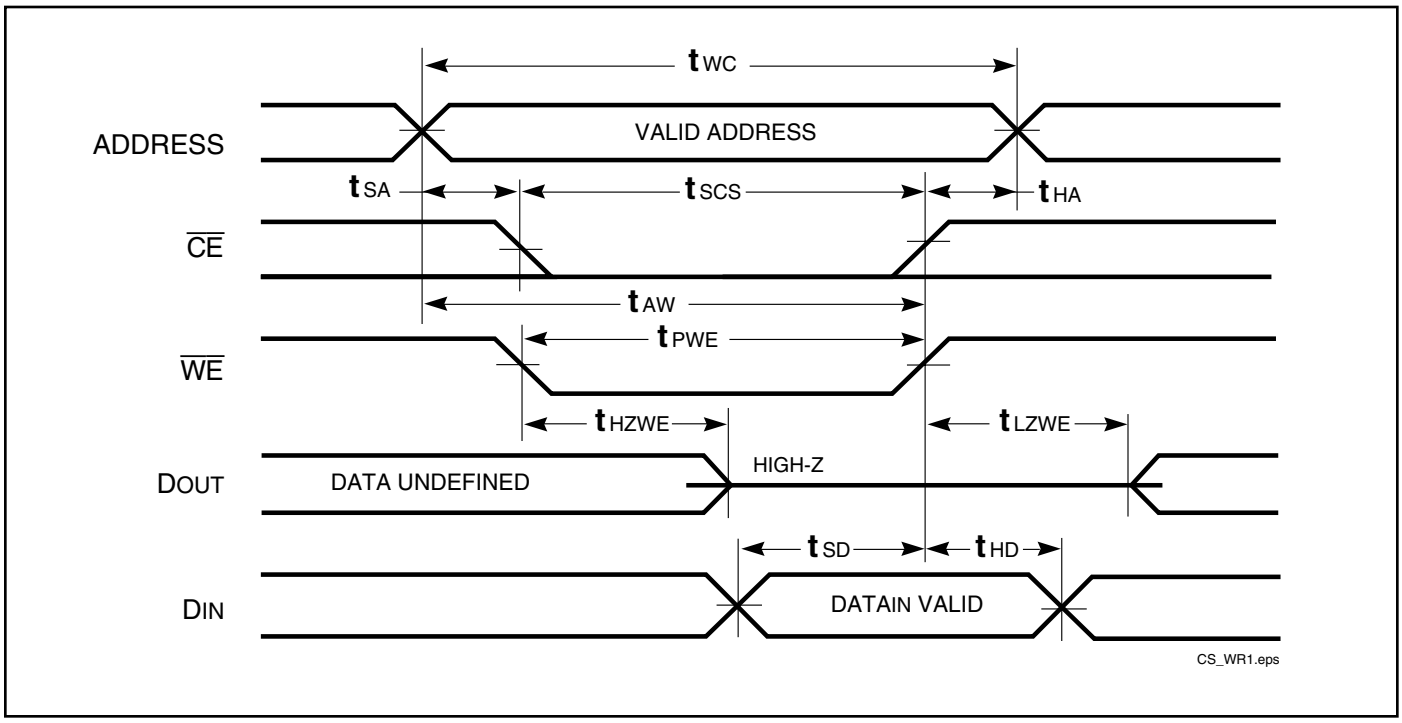
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-25 ns Min.	-25 ns Max.	-45 ns Min.	-45 ns Max.	Unit
t_{WC}	Write Cycle Time	25	—	45	—	ns
t_{SCS}	$\overline{CE}$ to Write End	15	—	35	—	ns
t_{AW}	Address Setup Time to Write End	15	—	25	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	15	—	25	—	ns
t_{SD}	Data Setup to Write End	12	—	20	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	8	—	20	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with $\overline{OE}$ HIGH.

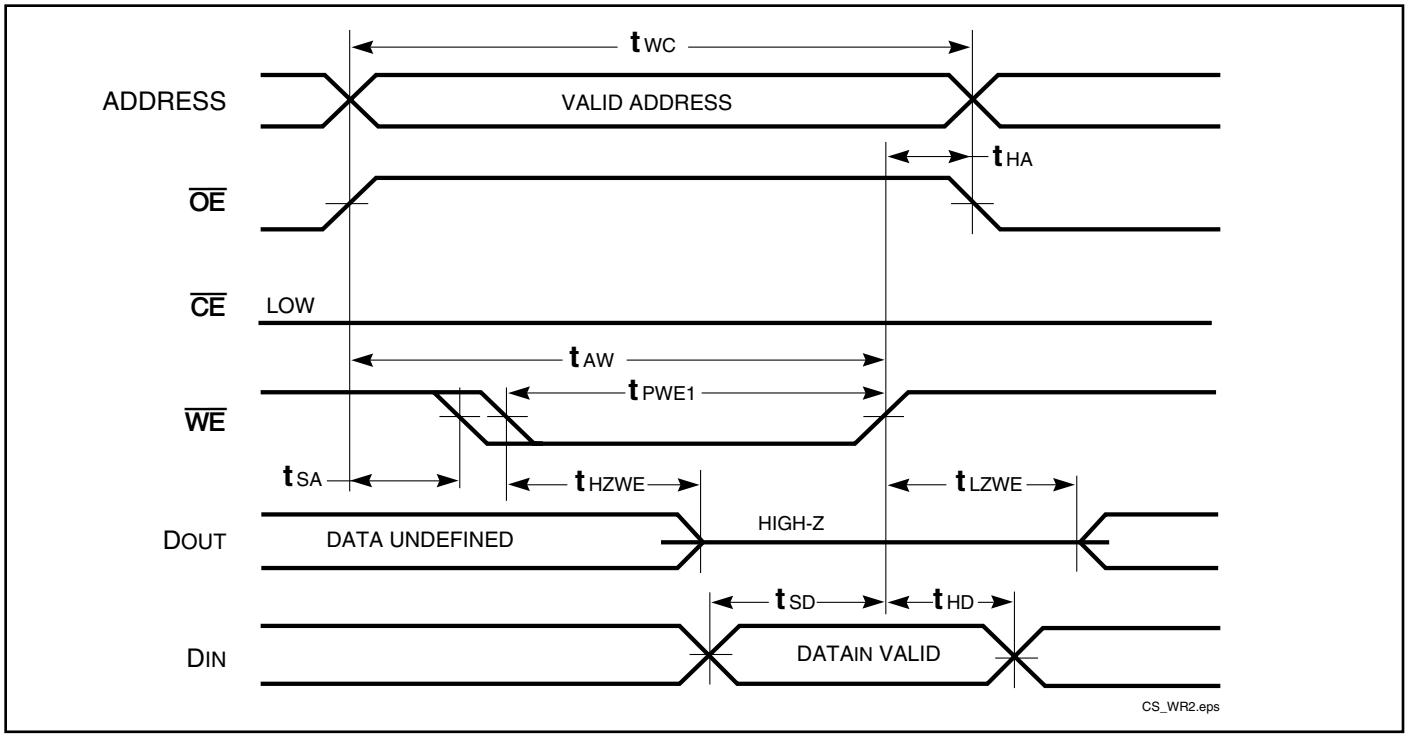
AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{CE}$ Controlled, $\overline{OE}$ is HIGH or LOW) [1]

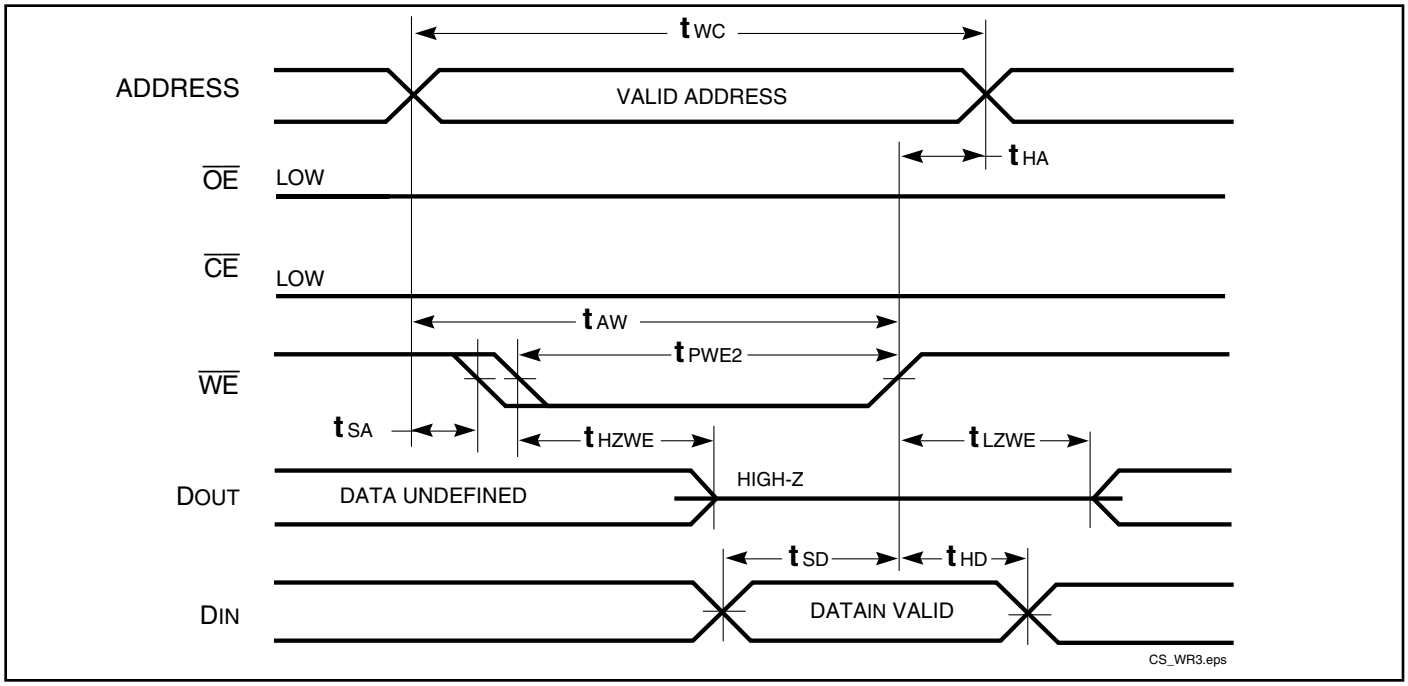


AC WAVEFORMS

WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) [1,2]



WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
2. I/O will assume the High-Z state if $\overline{OE}$ = V_{IH}.

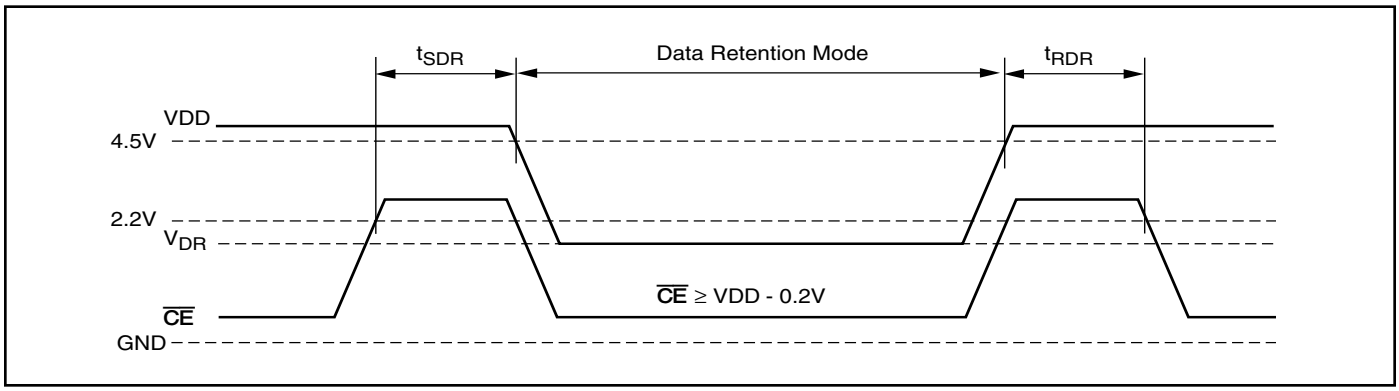
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0		5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	—	15	µA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—	—	20	
			Auto.	—	—	50	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

Note:

1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62C256AL-45TL	TSOP, Lead-free
	IS62C256AL-45UL	Plastic SOP, Lead-free

ORDERING INFORMATION

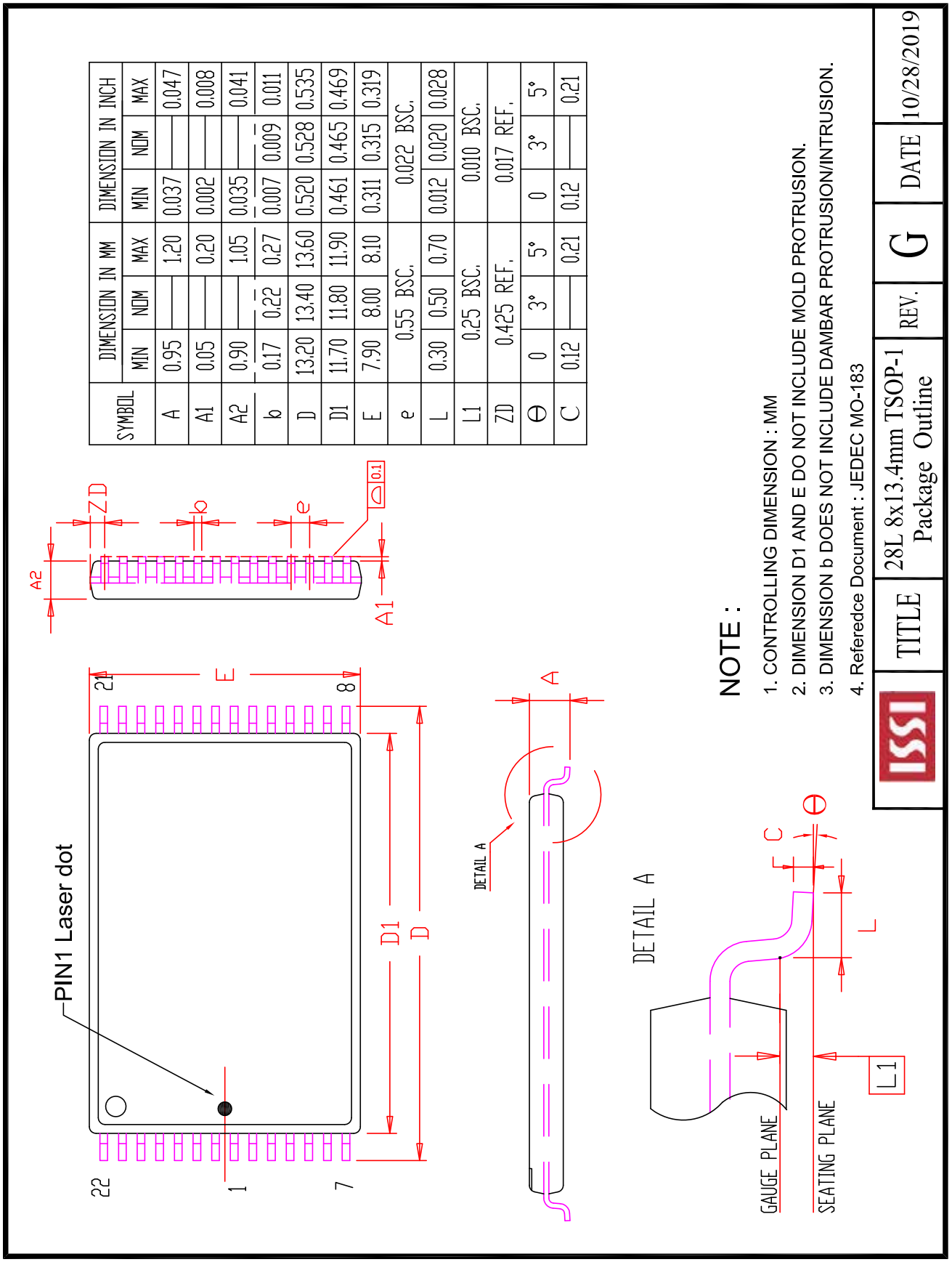
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
25	IS62C256AL-25ULI	Plastic SOP, Lead-free
45	IS62C256AL-45TLI	TSOP, Lead-free
	IS62C256AL-45ULI	Plastic SOP, Lead-free

ORDERING INFORMATION

Automotive Range: –40°C to +125°C

Speed (ns)	Order Part No.	Package
25	IS65C256AL-25TLA3	TSOP, Lead-free
	IS65C256AL-25ULA3	Plastic SOP, Lead-free
45	IS65C256AL-45TLA3	TSOP, Lead-free
	IS65C256AL-45ULA3	Plastic SOP, Lead-free



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.55	—	3.05	0.100	—	0.120
A1	0.05	—	0.35	0.002	—	0.014
b	0.35	—	0.50	0.014	—	0.020
D	17.70	—	18.62	0.697	—	0.733
E	11.50	—	12.70	0.453	—	0.500
E1	8.23	8.40	8.90	0.324	0.330	0.350
e	1.27 BSC.			0.050 BSC.		
L	0.40	—	1.27	0.016	—	0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.795 REF.			0.031 REF.		
θ	0	—	8°	0	—	8°

NOTE :
1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

ISSI	TITLE	28L 330mil SOP Package Outline	REV.	C	DATE	08/19/2009