

Features

Gain-bandwidth Product: 10 MHz
 Low Noise: 8.2 nV/√Hz(f= 1 kHz)

• Slew Rate: 7 V/µs

Offset Voltage: 1 mV (max)

• EMIRR IN+: 88 dB(under 2.4 GHz)

• Low THD+N: 0.0005%

Supply Range: 2.2 V to 5.5 V

• Supply Current: 1.4 mA/ch

• Low Input Bias Current: 0.3 pA Typical

· Rail-to-Rail I/O

• High Output Current: 70 mA (1.0 V Drop)

Applications

- · Sensor Signal Conditioning
- · Consumer Audio
- · Multi-Pole Active Filters
- Control-Loop Amplifiers
- · Communications
- Security
- Scanners

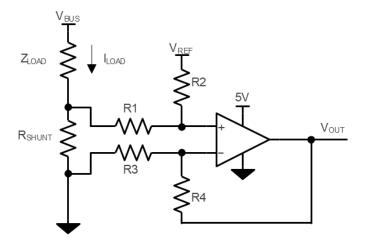
Description

The TP2411, TP2412, and TP2414 are low-cost, single, dual, and quad rail-to-rail output, single-supply amplifiers featuring low offset and input voltages, low-current noise, and wide signal bandwidth. The combination of low offset, low noise, very low input bias currents, and high speed make these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from this combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion of these devices.

Applications for these amplifiers include power amplifier (PA) controls, laser diode control loops, portable and loop-powered instrumentation, audio amplification for portable devices, and ASIC input and output amplifiers.

The TP2411 is the single-channel version available in 8-pin SOP and 5-pin SOT23 packages. The TP2412 is the dual-channel version available in 8-pin SOP, SOT, TSSOP, and MSOP packages. The TP2414 is the quad-channel version available in 14-pin SOP and TSSOP packages.

Typical Application Circuit



 $V_{OUT} = (I_{LOAD} \times R_{SHUNT}) \times (R2/R1) + V_{REF}$

When R3 = R1, R2 = R4, $R_{SHUNT} \ll R1$



Table of Contents

Features	
Applications	1
Description	1
Typical Application Circuit	1
Revision History	3
Pin Configuration and Functions	4
Specifications	
Absolute Maximum Ratings ⁽¹⁾	7
ESD, Electrostatic Discharge Protection	7
Thermal Information	7
Electrical Characteristics	8
Typical Performance Characteristics	10
Detailed Description	14
Overview	14
Functional Block Diagram	14
Application and Implementation	15
Low Side Current Sensing Application	15
Power Supply Recommendations	15
Tape and Reel Information	16
Package Outline Dimensions	17
SOT23-5	17
SOT23-8	18
SOP8	19
MSOP8	
TSSOP8	21
TSSOP14	22
SOP14	23
Order Information	24



Revision History

Date	Revision	Notes
2022/04/30 Rev.B.5 Updated order information.		
2022/07/18	Rev.B.6	Updated to new document format.
		Updated package dimensions.
2022/08/09 Rev.B.7		Correct typo error of MSL level, no product change.



Pin Configuration and Functions

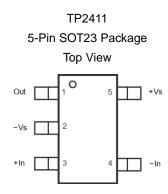


Table 6-1. Pin Functions: TP2411

Pin	Nama	1/0	Description			
SOT23	Name	I/O	Description			
1	Out	Output	Output			
2	-Vs		Negative power supply			
3	+In	Input	Noninverting input			
4	-In	Input	Inverting input			
5	+Vs		Positive power supply			



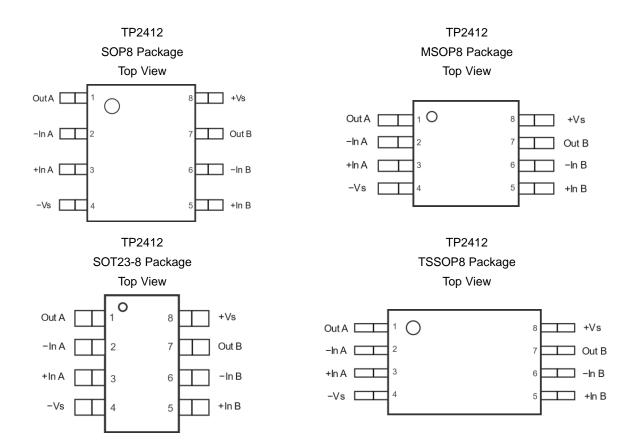


Table 6-2. Pin Functions: TP2412

Pin	Name	1/0	Description
1	Out A	Output	Output
2	−In A	Input	Inverting input
3	+In A	Input	Noninverting input
4	-Vs		Negative power supply
5	+In B	Input	Noninverting input
6	−In B	Input	Inverting input
7	Out B	Output	Output
8	+Vs		Positive power supply



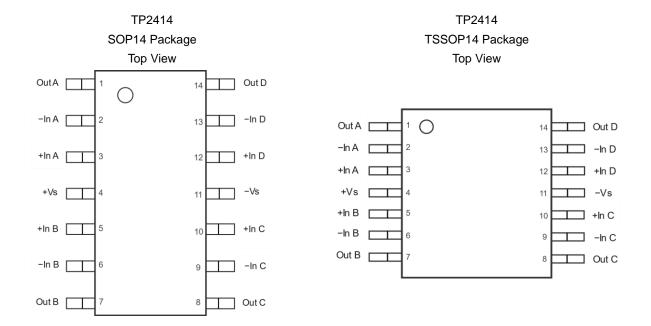


Table 6-3. Pin Functions: TP2414

Pin	Name	I/O	Description
1	Out A	Output	Output
2	−In A	Input	Inverting input
3	+In A	Input	Noninverting input
4	+Vs		Positive power supply
5	+In B	Input	Noninverting input
6	−In B	Input	Inverting input
7	Out B	Output	Output
8	Out C	Output	Output
9	−In C	Input	Inverting input
10	+In C	Input	Noninverting input
11	-Vs		Negative power supply
12	+In D	Input	Noninverting input
13	−In D	Input	Inverting input
14	Out D	Output	Output



Specifications

Absolute Maximum Ratings(1)

	Parameter	Min	Max	Unit
	Supply Voltage: V+ - V ⁻⁽²⁾		7	V
Input Voltage		V ⁻ - 0.3	V++ 0.3	V
Input Current: +IN, -IN ⁽³⁾		-20	+20	mA
	Output Short-Circuit Duration ⁽⁴⁾		Indefinite	
	Current at Supply Pins	-60	+60	mA
TJ	Maximum Junction Temperature		150	°C
T _A	Operating Temperature Range	-40	125	°C
T _{STG}	Storage Temperature Range	-65	150	°C
TL	Lead Temperature (Soldering 10 sec)		260	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1	kV

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	Ө ЈА	Ө лс	Unit
SOT23-5	250	81	°C/W
SOP8	158	43	°C/W
MSOP8	210	45	°C/W
TSSOP8	191	50	°C/W
SOT23-8	196	70	°C/W
SOP14	120	36	°C/W
TSSOP14	180	35	°C/W

⁽²⁾ The op amp supplies must be established simultaneously, with, or before, the application of any input signals.

⁽³⁾ The inputs and outputs are protected by ESD protection diodes to the negative power supply. If the input or output extends more than 500 mV beyond the negative power supply, the current should be limited to less than 10 mA.

⁽⁴⁾ A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many comparators are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



Electrical Characteristics

All test condition is T_A = 27°C. V_S = 5 V, R_L = 2 k Ω , C_L =100 pF, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
\/	Innut Offact Valtage	V _{CM} = V _S /2	-1	±0.25	+1	mV
Vos	Input Offset Voltage	V _{CM} = 0V	-1	±0.25	+1	mV
V _{os} TC	Input Offset Voltage Drift	-40°C to 125°C		1		μV/°C
		T _A = 27 °C		0.3		pА
lΒ	Input Bias Current	T _A = 85 °C		150		pА
		T _A = 125 °C		300		pА
los	Input Offset Current			0.3		pА
Vn	Input Voltage Noise	f = 0.1 Hz to 10 Hz		3.14		μV _{PP}
e n	Input Voltage Noise Density	f = 1 kHz		8.2		nV/√H z
in	Input Current Noise	f = 1 kHz		2		fA/√H z
Cin	Input Capacitance	Differential Common Mode		8 7		pF
		V _{CM} = 2.5 V	90	106		dB
CMRR	Common Mode Rejection Ratio	V _{CM} = 0 V to 3 V	80	106		dB
		V _{CM} = 0 V to 5 V	55	72		dB
Vсм	Common-mode Input Voltage Range		V 0.1		V++ 0.1	V
PSRR	Power Supply Rejection Ratio	Vs = 2.2 V to 5.5 V, V _{CM} = 0 V	82	100		dB
Avol	Open-Loop Large Signal Gain	$R_{LOAD} = 2 \text{ k}\Omega$, $V_{OUT} = -2 \text{ V to 2 V}$	100	120		dB
V _{OL} , V _{OH}	Output Swing from Supply Rail	$R_{LOAD} = 2 \text{ k}\Omega$		20	50	mV
Rout	Closed-Loop Output Impedance	G = 1, f =1 MHz, I _{OUT} = 0		0.2		Ω
Ro	Open-Loop Output Impedance	f = 1 kHz, lout = 0		125		Ω
Isc	Output Short-Circuit Current	Sink or source current	100	130		mA
Vs	Supply Voltage		2.2		5.5	V
ΙQ	Quiescent Current per Amplifier	Vs = 5 V		1.4	1.95	mA
PM	Phase Margin	$R_{LOAD} = 1 \text{ k}\Omega, C_{LOAD} = 60 \text{ pF}$		60		0
GM	Gain Margin	$R_{LOAD} = 1 \text{ k}\Omega, C_{LOAD} = 60 \text{ pF}$		8		dB
GBWP	Gain-Bandwidth Product	f = 1kHz		10		MHz
SR	Slew Rate	$A_V = 1$, $C_{LOAD} = 100$ pF, $R_{LOAD} = 2$ k Ω	3.0	7		V/µs



FPBW	Full Power Bandwidth Note 1		414	kHz
ts	Settling Time, 0.1% Settling Time, 0.01%	A _V = -1, 1 V Step	0.75 0.85	μs
THD+N	Total Harmonic Distortion and Noise	$f = 1 \text{ kHz}, A_V = 1, R_{LOAD} = 2 \text{ k}\Omega,$ $V_{OUT} = 1 \text{Vp-p}$	0.0005	%
X _{talk}	Channel Separation	$f = 1 \text{ kHz}, R_L = 2 \text{ k}\Omega$	110	dB

⁽¹⁾ Full power bandwidth is calculated from the slew rate FPBW = $SR/\pi \cdot VP-P$.

Typical Performance Characteristics

 $V_S = \pm 2.75 \text{ V}$, $V_{CM} = 0 \text{ V}$, $R_L = \text{Open}$, unless otherwise specified.

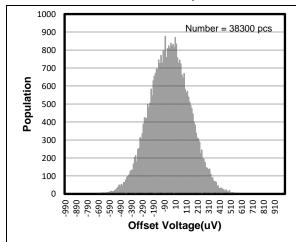


Figure 1. Offset Voltage Production Distribution

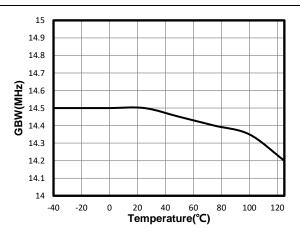


Figure 2. Unity Gain Bandwidth vs. Temperature

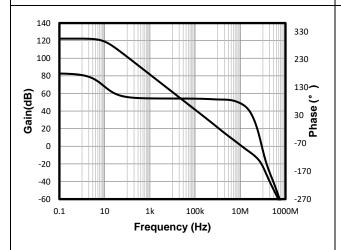


Figure 3. Open-Loop Gain and Phase

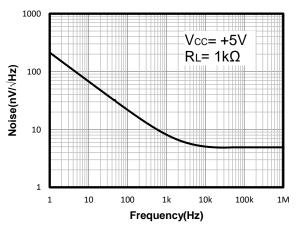


Figure 4. Input Voltage Noise Spectral Density

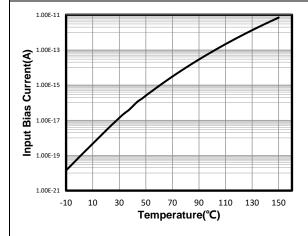


Figure 5. Input Bias Current vs. Temperature

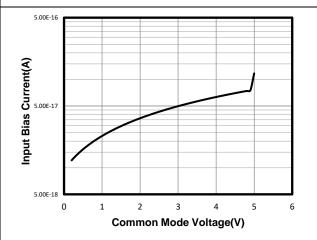
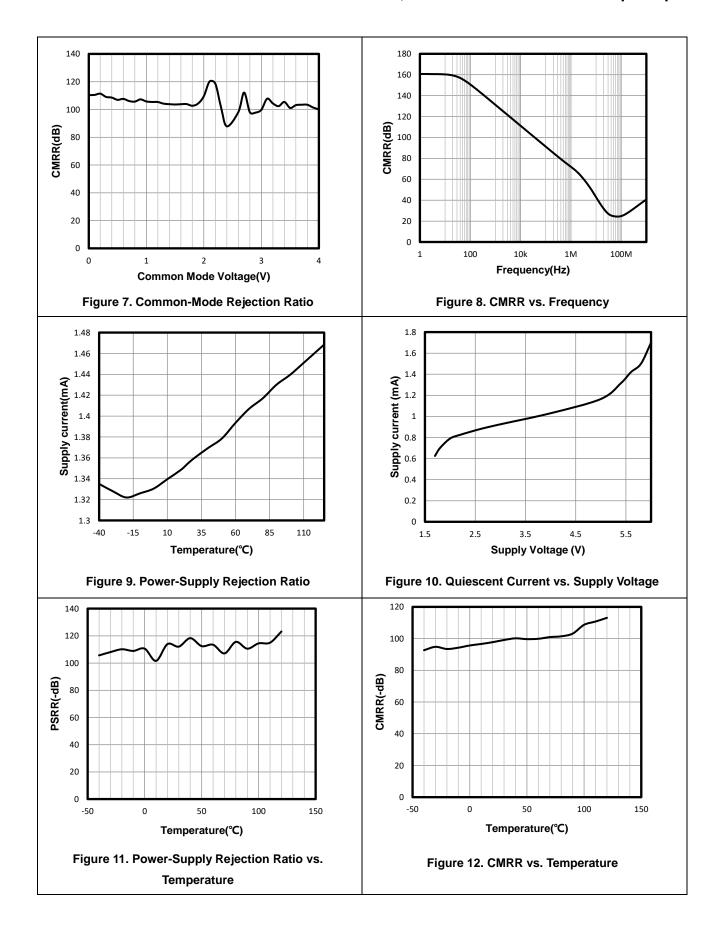
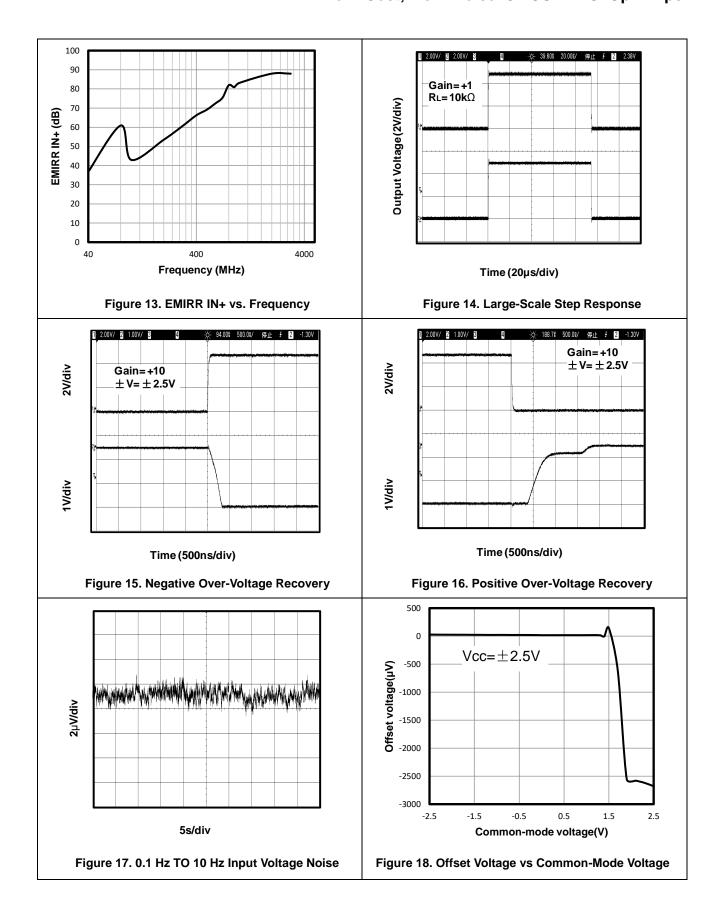


Figure 6. Input Bias Current vs. Common-Mode Voltage

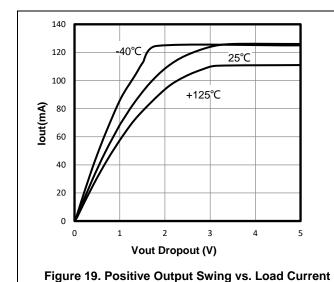


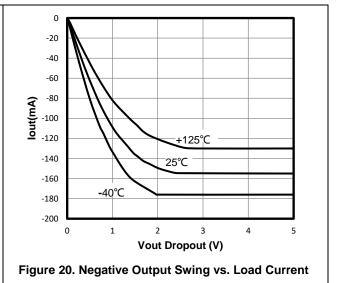












www.3peakic.com.cn 13 / 24 Rev.B.7



Detailed Description

Overview

The TP2411 series op amps can operate on a single-supply voltage (2.2 V to 5.5 V), or a split-supply voltage (± 1.1 V to ± 2.75 V), making them highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001 μ F to 0.1 μ F). These amplifiers are fully specified from ± 2.2 V to ± 5.5 V and over the extended temperature range of ± 40 °C to ± 125 °C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

Functional Block Diagram

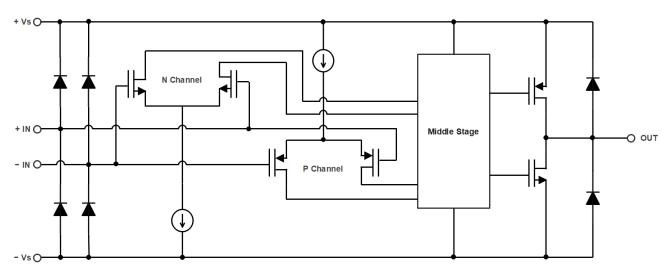


Figure 21. Functional Block Diagram

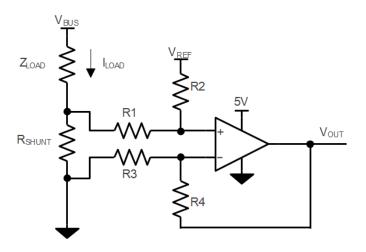
Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Low Side Current Sensing Application

Figure 22 shows the TP241X configured in a low-side current sensing application. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The voltage dropping across the resistor is amplified by different amplifier circuits with TP241X. The V_{REF} can be used to add bias voltage to output voltage. Particular attention must be paid to the matching and precision of R1, R2, R3, and R4, to maximize the accuracy of the measurement.



 $V_{OUT} = (I_{LOAD} \times R_{SHUNT}) \times (R2 / R1) + V_{REF}$ When R3 = R1, R2 = R4, R_{SHUNT} << R1

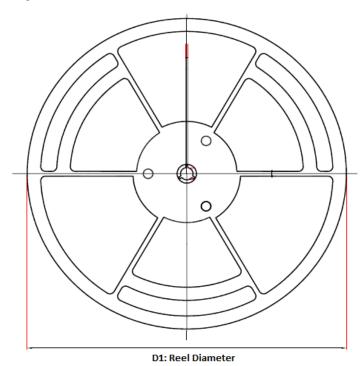
Figure 22 Dual Supply Operation Connections

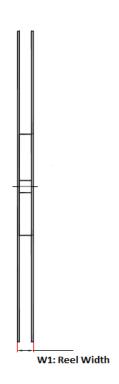
Power Supply Recommendations

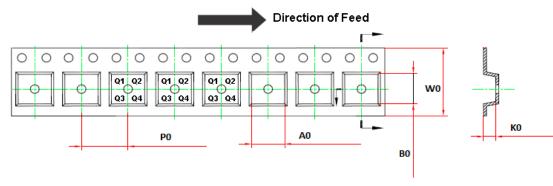
Place 0.1-µF bypass capacitors close to the power supply pins for reducing coupling errors from the noisy or high impedance power supplies.



Tape and Reel Information







Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TP2411-TR	SOT23-5	180.0	13.1	3.2	3.2	1.4	4.0	8.0	Q3
TP2412-SR	SOP8	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TP2412-VR	MSOP8	330.0	17.6	5.2	3.3	1.5	8.0	12.0	Q1
TP2412-TR	SOT23-8	178.0	12.3	3.2	3.2	1.4	4.0	8.0	Q3
TP2412-TSR	TSSOP8	330.0	17.6	6.8	3.3	1.2	8.0	12.0	Q1
TP2414-SR	SOP14	330.0	21.6	6.5	9.0	2.1	8.0	16.0	Q1
TP2414-TR	TSSOP14	330.0	17.6	6.8	5.4	1.2	8.0	12.0	Q1



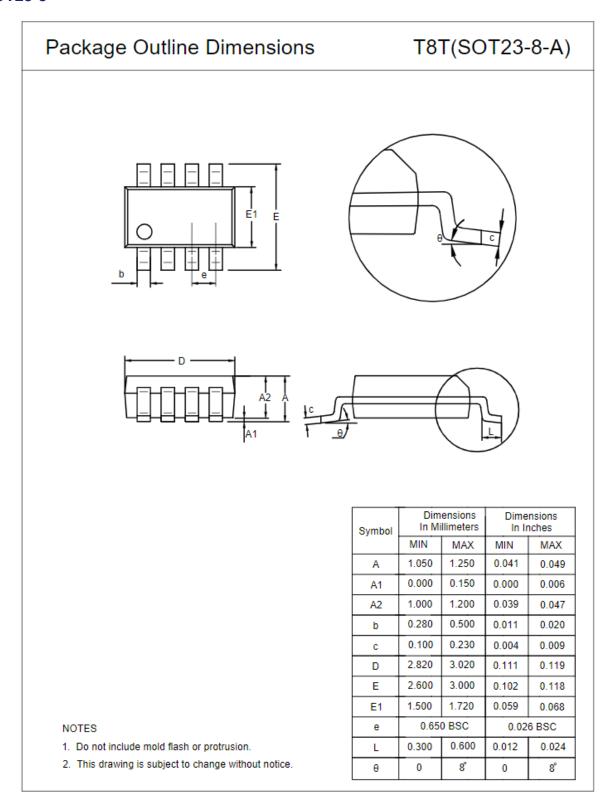
Package Outline Dimensions SOT23-5

Package Outline Dimensions S5T(SOT23-5-A) Dimensions Dimensions In Millimeters Symbol In Inches MIN MAX MIN MAX 1.050 1.250 0.041 0.049 0.000 0.150 0.000 0.006 1.000 A2 1.200 0.039 0.047 0.280 0.500 0.011 0.020 0.100 0.230 0.004 0.009 2.820 3.020 0.111 0.119 D 2.600 3.000 Ε 0.102 0.118 1.500 1.720 0.059 E1 0.068 0.950 BSC 0.037 BSC NOTES 0.300 0.600 1. Do not include mold flash or protrusion. 0.012 0.024 2. This drawing is subject to change without notice. 8 0 0 8°

www.3peakic.com.cn 17 / 24 Rev.B.7

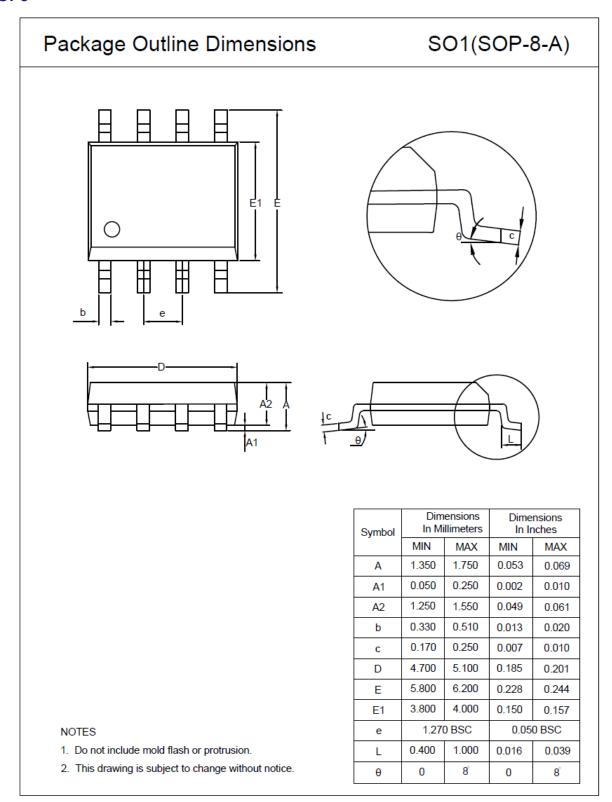


SOT23-8



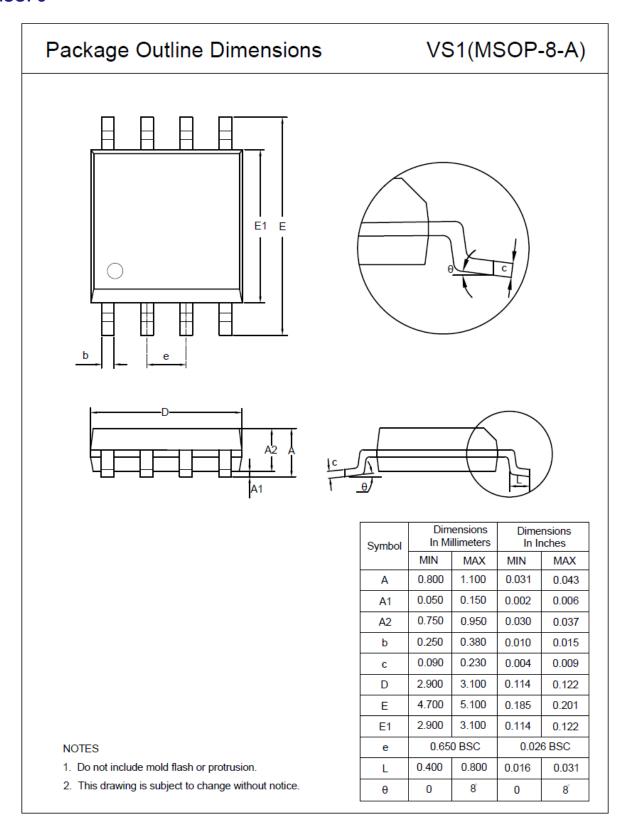


SOP8



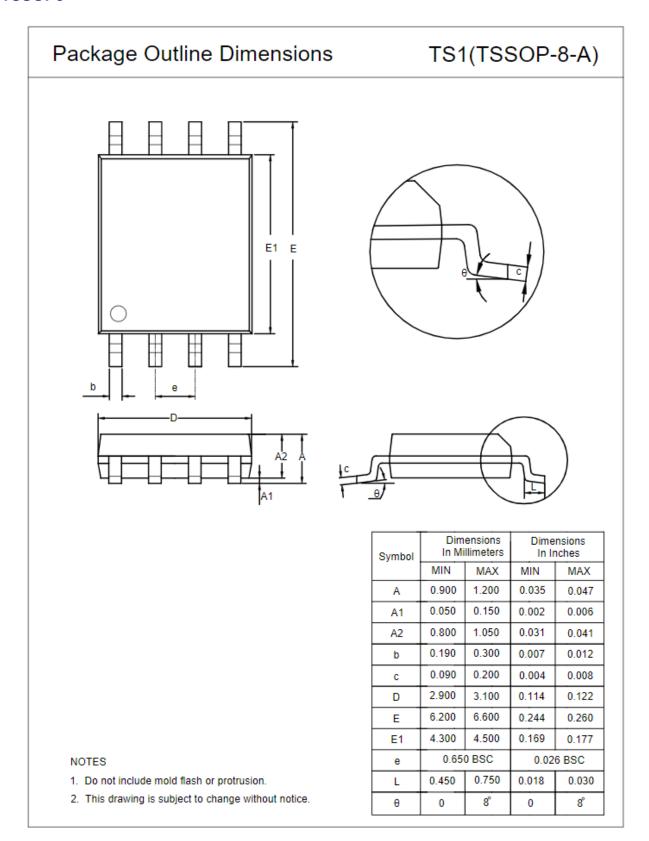


MSOP8



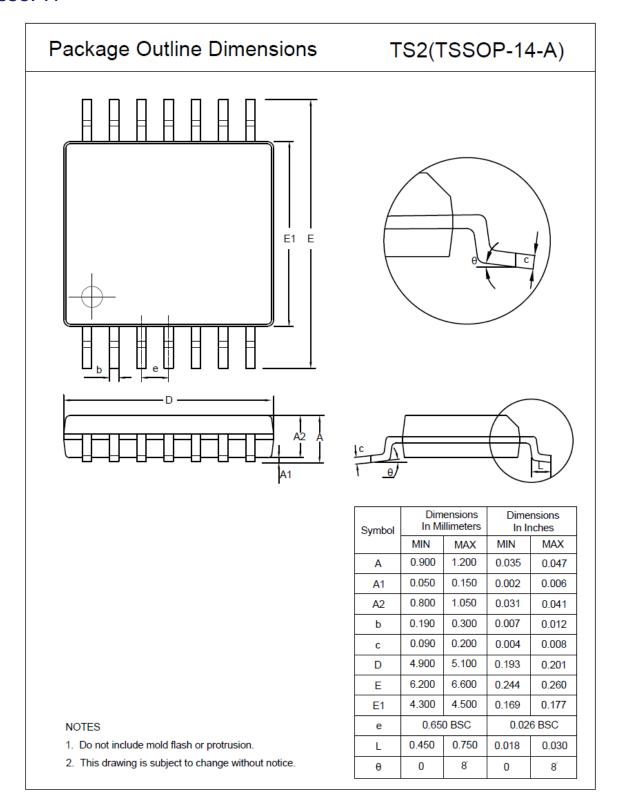


TSSOP8



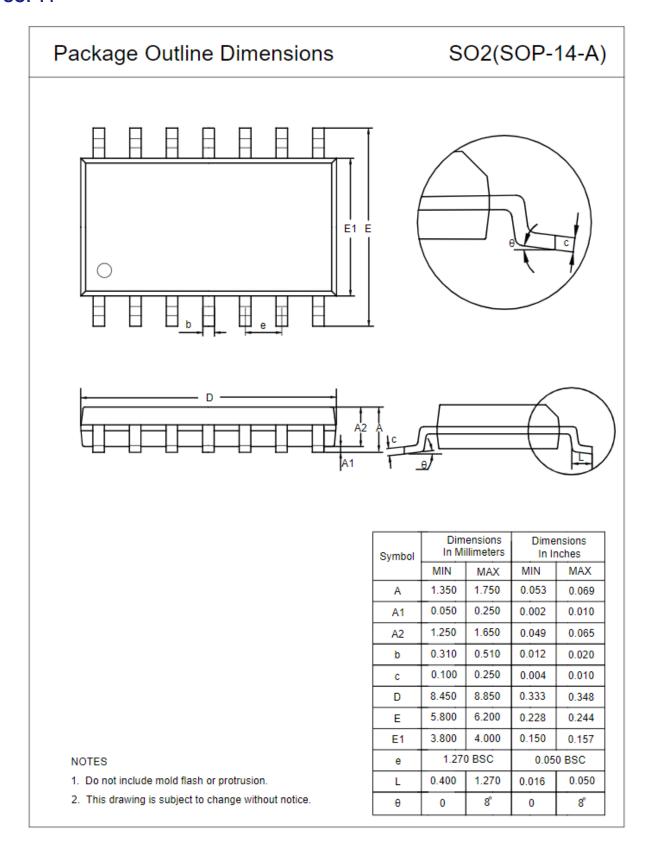


TSSOP14





SOP14





Low Cost, Low Noise

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transpor Quar
TP2411-TR	-40 to 125°C	SOT23-5	411	3	Tape and R
TP2412-SR	-40 to 125°C	SOP8	TP2412	3	Tape and R
TP2412-VR	-40 to 125°C	MSOP8	TP2412	3	Tape and R
TP2412-TSR	-40 to 125°C	TSSOP8	TP2412	3	Tape and R
TP2412-TR	-40 to 125°C	SOT23-8	S12	3	Tape and R
TP2414-SR	-40 to 125°C	SOP14	TP2414	3	Tape and R
TP2414-TR	-40 to 125°C	TSSOP14	TP2414	3	Tape and R

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

³PEAK and the 3PEAK logo are registered trademarks of 3PEAK INCORPORATED. All of property of their respective owners.